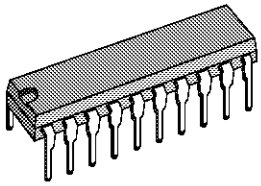
SGS-THOMSON MICROELECTRONICS

L6720
L6721

MINITEL INTERFACE

ADVANCE DATA

- ONE NON INVERTING LINE DRIVER
- ONE NON INVERTING LINE RECEIVER
- LINE TRANSCEIVER: (TOWARDS PERIPHERALS)
  - non inverter from Minitel to peripherals
  - inverter from peripherals to Minitel
- POWER SUPPLY
  - not regolated output voltage
  - internal low drop power switch with antisaturation circuit
  - output protected against short circuit
  - standby mode operation with an external signal
- AUDIO AMPLIFIER
  - one input, one output
  - one pin for supply rejection
  - internal fixed gain
- THERMAL SHUTDOWN



Powerdip 16+2+2

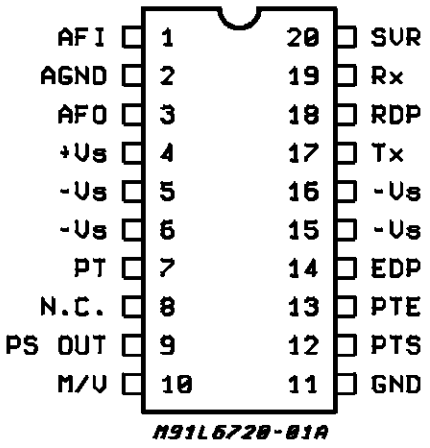
ORDERING NUMERS: L6720
L6721

DESCRIPTION

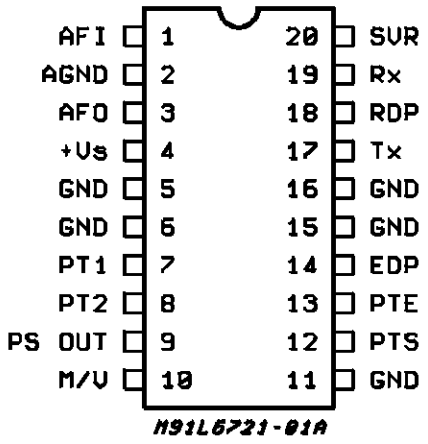
This device performs the functions of a complete interface for Minitel peripheral plug.

It integrates one line driver, one line receiver, one line transceiver, a power supply for peripherals, and an audio amplifier, Two version are provided:
- L6720 which needs a negative supply.
- L6721 which doesn't use a negative supply.

PIN CONNECTIONS

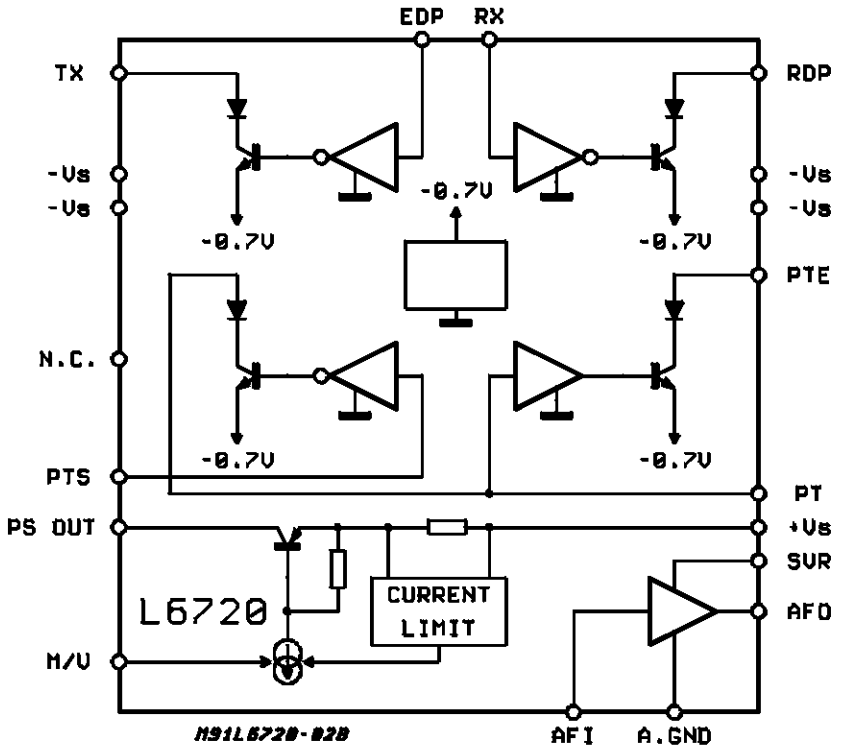


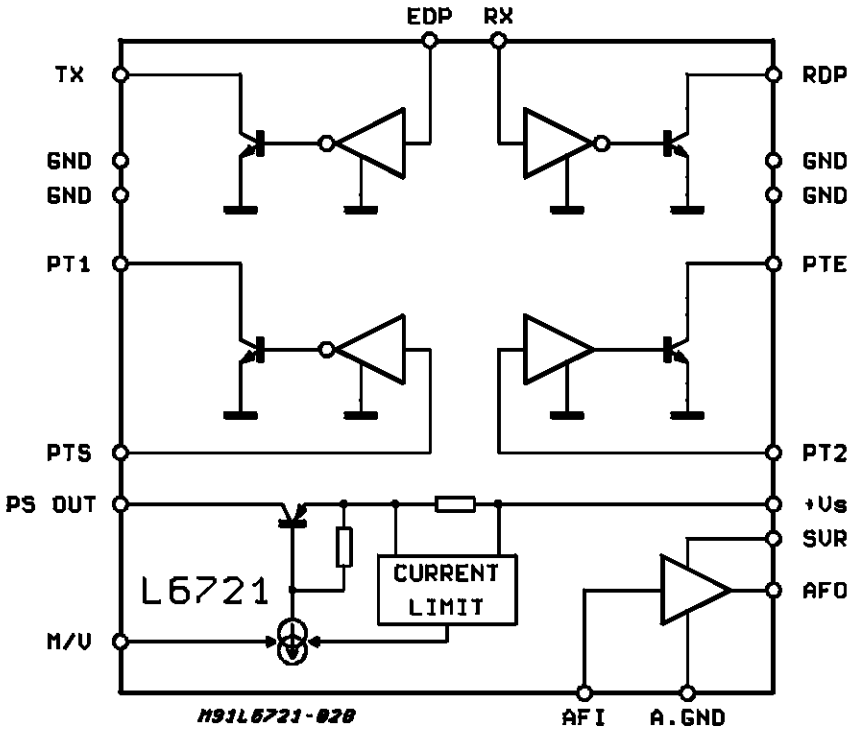
L6720



L6721

BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
$+V_S$,(V_S)	Positive Supply Voltage	+15	V
$-V_S$	Negative Supply Voltage	-13	V
V_{OC}	Open Collectors Voltage	max 20	V
I_{OC}	Open Collectors Current	max 10	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70°C	1.25	W
T_J	Junction Temperature	150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

THERMAL DATA

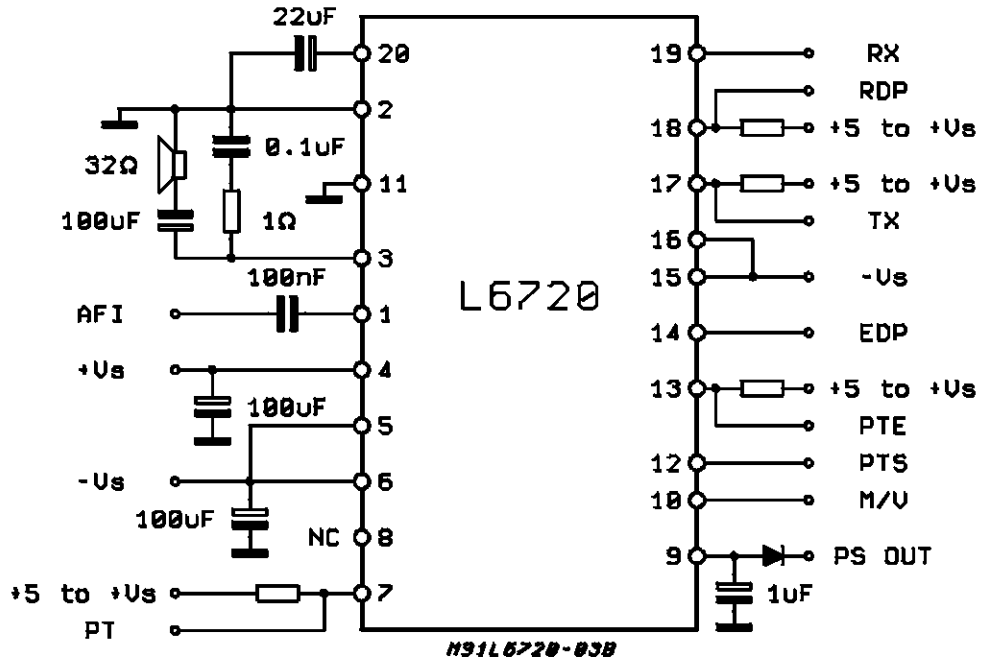
Symbol	Description		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	14	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	(*)65	°C/W

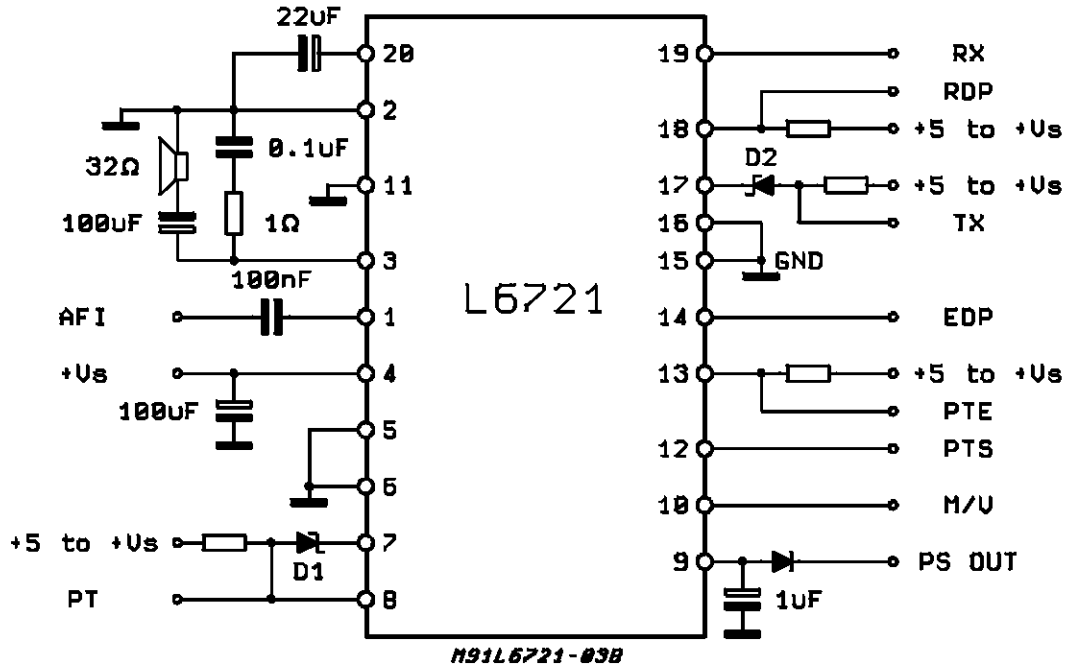
(*) Mounted on board with minimized dissipating copper area

PIN FUNCTIONS

Pin	Name	Function
1	AFI	Audio Frequency input
2	AGND	Audio Amplifier Ground
3	AFO	Audio amplifier output
4	$+V_S$,(V_S)	Power Supply Input (to plug)
5	$-V_S$,(GND)	Negative Supply (GND for L6721)
6	$-V_S$,(GND)	Negative Supply (GND for L6721)
7	PT	Transceiver Input/Output (L6720)
8	N.C.	Not Connected (L6720)
7	PT1	Transceiver Output (to plug) (L6721)
8	PT2	Transceiver Input (from plug) (L6721)
9	PSout	Power Supply Output (to plug)
10	M/V	Inhibition of peripheral output power
11	GND	Ground pin
12	PTS	Line Transceiver Input (from Minitel)
13	PTE	Line Transceiver Output (to Minitel)
14	EDP	Line Driver Input (from Minitel)
15	$-V_S$,(GND)	Negative Supply (GND for L6721)
16	$-V_S$,(GND)	Negative Supply (GND for L6721)
17	T_X	Line Driver Output (to plug)
18	RDP	Line Receiver Output (to Minitel)
19	R_X	Line Receiver Input
20	SVR	Supply Voltage Rejection

APPLICATION DIAGRAMS





D1-D2: SCHOTTKY VF ≤ 0.3V at 10mA
VR = 20Vmin

ELECTRICAL CHARACTERISTICS

I) LINE DRIVER, LINE RECEIVER, LINE TRANCEIVER

L6720: with negative supply

Test Conditions: $10V < +V_S < 12V$, $-8V <- V_S < -4V$, $T_j = 25°C$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level (Pins Rx, EDP, PTS, PT)				0.8	V
V_{IH}	Input High Level (pins Rx, EDP, PTS, PT)		2			V
I_G	Pull-up Current Generator on Pins Rx, PT		160	250	340	µA
Z_I	Input Impedance on pins Rx, Tx, PT	Pins V_S and $-V_S$ open	68			KΩ
V_{OL}	Output Low Level (pins Tx, PT, PTE)	I_{LOAD} = 6mA			0.4	V
I_R	Output Leakage Current (pins Tx, RDP, PTE)				10	µA
t_{PLH}, t_{PHL}	Propagation Delay Time	I_{LOAD} = 6mA C_{out} = 50pF		3	5	µs
t_r, t_f	Output Rise and Fall Time			1		µs

L6721: without negative supply

Test Conditions: $10V < V_S < 12V$, $T_j = 25°C$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level (Pins Rx, EDP, PTS, PT2)				0.8	V
V_{IH}	Input High Level (pins Rx, EDP, PTS, PT2)		2			V
I_G	Pull-up Current Generator on Pins Rx, PT2		160	250	340	µA
Z_I	Input Impedance on pins Rx, Tx, PT2	Pins V_S and GND open	68			KΩ
V_{OL}	Output Low Level (pins Tx, PT1)	I_{LOAD} = 6mA			0.15	V
V_{OL}	Output Low Level (pins RDP, PTE)	I_{LOAD} = 6mA			0.4	V
I_R	Output Leakage Current (pins Tx, RDP, PT1, PTE)				10	µA
t_{PLH}, t_{PHL}	Propagation Delay Time	I_{LOAD} = 6mA C_{out} = 50pF		3	5	µs
t_r, t_f	Output Rise and Fall Time	I_{LOAD} = 6mA C_{out} = 50pF		1		µs

II) POWER SUPPLY

L6720: $+V_S = 12V$, $-V_S = -8V$
L6721: $V_S = 12V$
$T_j = 25°C$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_I - V_O$	Dropout Voltage	I_{LOAD} = 1A		0.4	0.8	V
I_{SC}	Short Circuit Current		1	1.1	1.2	A
M/V_L	Low Level Disable Pin (1)				0.8	V
M/V_H	High Level Disable Pin (1)		2			V
I_L	Disable Pin Input Current	M/V = 0			100	µA
I_Q	Quiescent Current	I_{LOAD} = 1A I_{LOAD} = 0.25A			60 23	mA mA

Note (1) Power supply is disabled when a zero level voltage is applied on M/V Pin

III) AUDIO AMPLIFIER (2)

L6720: $+V_S$ = 12V, $-V_S$ = -8V
L6721: V_S = 12V
T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_i	Input Impedance		20			KΩ
AV	Voltage Gain		28	30	32	dB
BW	Bandwidth		10			KHz
P_O	Output Power	Distortion = 10%, f = 1KHz R_{LOAD} = 32Ω, 10V < V_{CC} < 14V	250			mW

Note (2): The output of the audio amplifier is protected against short circuits toward positive power supply and ground

IV) PROTECTIONS

1) L6720 (With negative supply)

Pins Rx, Tx, PT are protected against any DC voltage ranging from -18V to +18V, with the device supplied or not, without extra components.

2) L6721 (Without negative supply)

Pins Tx, PT1 are not protected: an external schottky diode must be added to protect them from -18V to +18V (see application diagram).
Pins Rx, PT2 are protected against any DC voltage ranging from -18V to +18V.

3) In Both Options

P. Supply pin is not protected: an external diode must be inserted to protect it (see application diagram).
The suggested electrical characteristic of the external diode are:

- $V_{REVERSE}$ > 20V
- Voltage drop at 1A max. 1.2V

4) Thermal Protection

This protection is operating when the chip temperature typically raises above 150°C (hysteresis 20°C Typ; this indicated value is valid with the application circuit on pag. 4), turning off both the power switch and the audio amplifier.

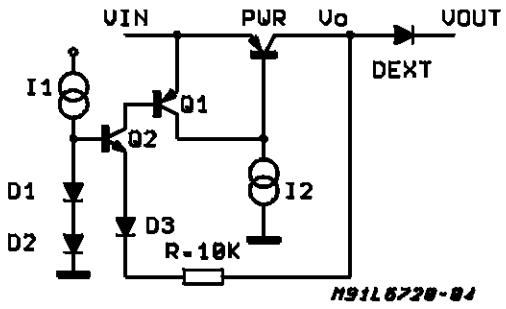
APPLICATION INFORMATION

The external diode on the output of the power switch has the fundamental function of protecting this pin against positive overvoltages.

However the voltage drop on this diode is also important in the correct definition of the thermal hysteresis. This can be understood by considering the circuit applied on the output of the power switch, which has the function of withstanding negative overvoltages.

Let's refer to fig. 1:

Figure 1



D_{EXT}: EXTERNAL DIODE; PWR: POWER TRANSISTOR; I_1, I_2: CURRENT GENERATORS; R: RESISTANCE; D1, D2, D3: DIODES; Q1, Q2: SIGNAL TRANSISTORS

When V_{OUT} = 0.7V Q2 and D3 turn on and also Q1 whose saturation turns off the power PWR. In this condition (BV_{CBO}) it can withstand the maximum negative overvoltage (-18V).

If we now have an overload on V_{OUT} (after the diode) for example with V_{IN} = 12V, V_{OUT} = 8V, P_d = 4W, the temperature of the chip increases to the thermal shutdown intervention, so that V_{OUT} = 0. However Q1 and Q2 cannot turn on because we have 2 diodes (D1 and D2) against 3 diodes (D3, D_{EXT}, Base-Emitter of Q2).
If the over load is on point V_O (before the external diode) as before the chip temperature increases until shutdown. But in that condition (with V_{OUT} = 0) we have now 2 diodes (D1, D2) against other 2 diodes (D3, Q2 Base-Emitter); than the power switch doesn't turn on because of a slight difference between the thermal coefficient of the 4 diodes.

We will have the new switching-on of power switch only when the chip temperature decreases of about 80°C (being kept off by Q1 and Q2).

In conclusion with or without the external diode the absolute value of the thermal shutdown is the same, but the hysteresis is higher without the external diode.

THERMAL CHARACTERISTICS

The transient thermal resistance of the 16+2+2 powerdip package is shown in Fig. 2: a typical $R_{th\ j\text{-}amb}$ of 50° C/W roughly can be seen.To be able to well sink out the heast from the inside of the package, the four control pins can be closely connected to a p.c.b. copper side. By considering the two square sides of Fig. 4, the thermal resistance junction-ambient can be reduced according to Fig. 3.

Figure 2: DIP 16+2+2 Transient Thermal Resistance for single pulses.

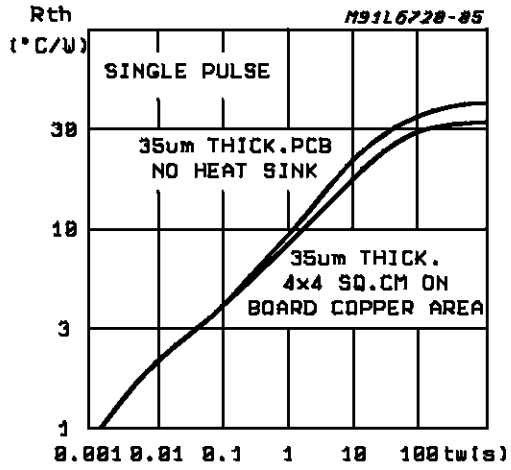


Figure 3: Typical R_{th} j-a of Powerdip 16+2+2 vs side 1 for heat sink on the PCB lower side.

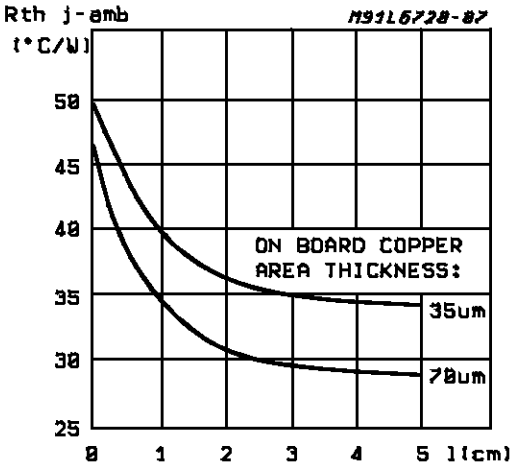
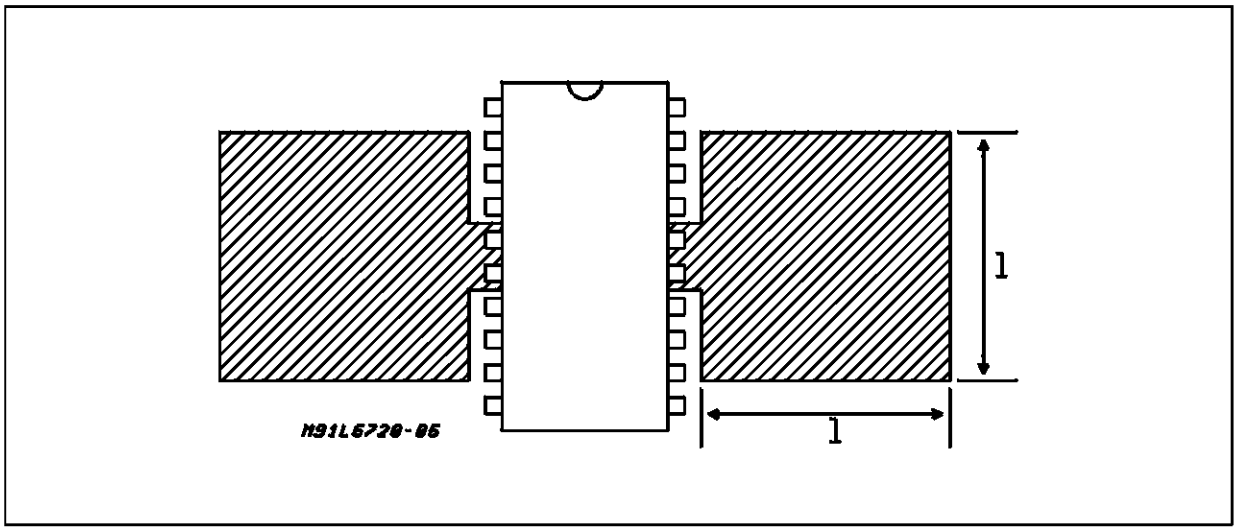


Figure 4: Two "On Board" square heat sink



POWERDIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050